An Ultra-Wideband MMIC Balanced Frequency Doubler Using Line-Unified HEMTs

Tsutomu Takenaka, *Member, IEEE,* and Hiroyo Ogawa, *Member, IEEE*

***Abstract*—A very small, ultra-wideband MMIC balanced frequency doubler, which employs line-unified HEMT configurations, is proposed. A chip size of 1.0 mm × 0.9 mm is achieved with a conversion loss of 8–10 dB in the 4–40 GHz output harmonics frequency range and fundamental frequency signal isolation of better than 21 dB above the input fundamental frequency of 7 GHz. Circuit parameters are optimized in a novel and simple prediction using an equation derived from HEMT's dc characteristic and a linear-state CAD software package. The doubler promises to realize miniaturized, wideband MMIC transmitters/receivers.**

I. Introduction

MICROWAVE and millimeter-wave frequency doublers often employ a balanced circuit configuration [1], [2] in order to provide good fundamental frequency signal suppression without fundamental frequency trapping stubs. The balanced frequency doublers basically separate fundamental signals out-of-phase and combine second harmonics in phase [3]. For these requirements, conventional balanced doublers use quarter-wavelength couplers or baluns which primarily determine the MIC or MMIC chip size and operating frequency range. Recently, distributed MMIC balanced frequency doublers have been reported [4], [5]. They realize wideband balanced operation on MMIC chips by using the phase shift difference between the common source FET (CSF) and common-gate FET (CGF), and distributed transmission lines. However, they still require large chip area given the number of FETs, transmission lines and inductors involved. Moreover, it is difficult to maintain balanced operation of the CSF and CGF [5], [6] above the output frequency of 20 GHz.

This paper proposes a very small MMIC balanced frequency doubler which operates in the 4–40 GHz output frequency range and utilizes line-unified FET configurations [7], [8]. In the line-unified FET configurations, copolanar lines such as slotlines and coplanar waveguides (CPW's) are effectively unified with the FET electrode locations by regarding some sets of FET parallel electrodes as a combination of several coplanar microwave transmission lines. The proposed doubler consists of a common-drain high-electron-mobility-field-effect-transistor (HEMT) unifying a slotline series T-junction as an out-of-phase divider [9], and a common-gate HEMT unifying a CPW and a slotline as a line-transition circuit from the CPW to the slotline. These line-unified HEMTs provide balanced doubler operation up to the HEMTs' cutoff frequency in an MMIC chip only 1.0 mm × 0.9 mm, owing to the absence of quarter-wavelength couplers, fundamental frequency trapping stubs and impedance matching stubs. The common-gate and drain HEMTs provide an active input and output impedance match [10], respectively. Advantages of the proposed balanced doubler are ultra-wideband circuit performance and remarkable chip size reduction.

In the design, we optimize circuit parameters by using an equation derived from HEMT's dc characteristic with a commercially available linear-state CAD software package (Touchstone). Since the conversion gain of the proposed doubler is given as a function of the linear-state insertion gain, the doubler's second harmonic frequency response is simply simulated in the linear-state analysis.

II. Configuration and Operation

The equivalent circuit diagram of the proposed balanced frequency doubler is shown in Fig. 1. The proposed doubler consists of three blocks. The first is a line-unified common-gate HEMT which shifts from CPW mode to slotline mode, and matches the impedance at input port①. The second consists of inductive lines (L_1, L_2) which compensate for bandwidth degradation due to parasitics in the HEMTs. The last is a line-unified common-drain HEMT unifying a slotline series T-junction and CPWs, which divides the fundamental signal out-of-phase, generates second harmonics, combines the second harmonics in phase and matches impedance at output port②.

The line-unified common-gate HEMT in Fig. 1, has an electrode configuration of drain (D_1)-gate (G_1)-source (S_1) as shown in Fig. 2. When the G_1 is used as a common electrode, a CPW and a slotline are formed in the G_1-S_1-G_1 and the D_1-G_1 structures, respectively. The input fundamental signal from the input port① CPW is transmitted to the slotline required in the next stage, accompanied by an impedance transition from low to high. Appropriate

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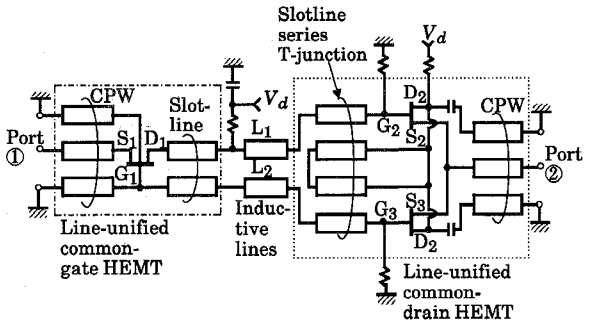


Fig. 1. Equivalent circuit diagram of the proposed balanced frequency doubler.

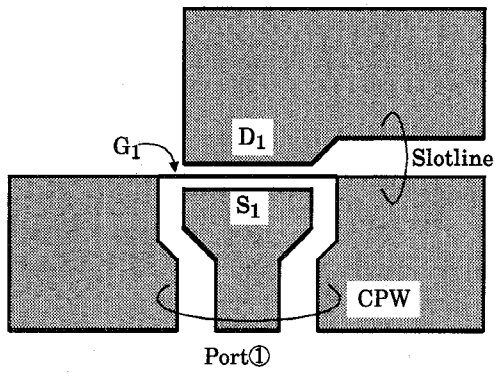


Fig. 2. Line-unified common-gate HEMT electrode configuration.

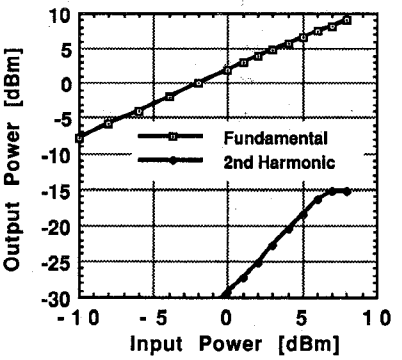


Fig. 3. Measured output power performance of the line-unified common-gate HEMT as a function of input power at 10 GHz fundamental frequency.

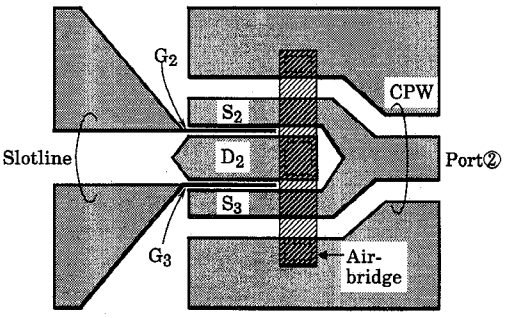
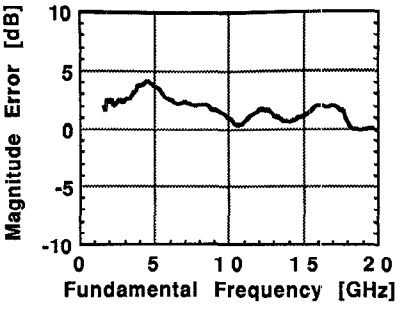


Fig. 4. Line-unified common-drain HEMT electrode configuration.

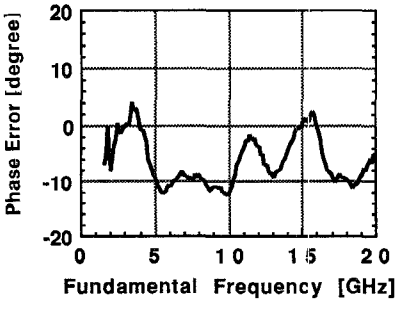
biasing of the gate-source circuit provides a small-signal active impedance match, $g_{m1}Z_0 = 1$ [6] in the linear state region, where g_{m1} and Z_0 are the transconductance of the common-gate HEMT and the normalized input port impedance at 50 Ω, respectively. Measured 10 GHz input versus output power performance of the common-gate HEMT shown in Fig. 2 is shown in Fig. 3. The input power at the 1 dB power compression point is 8 dBm, and the difference between fundamental and second harmonic signals is 24 dB at an input power of 6 dBm. Therefore, common-gate HEMT harmonics are negligible and a linear state operation can be assumed up to an input power of 6 dBm.

The line-unified common-drain HEMT enclosed by the dotted line in Fig. 1, has an electrode configuration of source (S_2)-gate (G_2)-drain (D_2)-gate (G_3)-source (S_3) as shown in Fig. 4. The relationship between the electrode strips is established by an air-bridge connecting the D_2 electrode strip to the outer conductors for output CPW port②. A slotline series T-junction, as the out-of-phase divider, is composed of the common-drain D_2 electrode and two gate G_2, G_3 electrodes, one on each side of the D_2 electrode. An in-phase combiner is formed by the two source electrodes S_2, S_3 which are connected to each other to act as a center conductor of output CPW port②. The fundamental signal from the slotline is divided out-of-phase in the slotline series T-junction, and fed to gates G_2 and G_3. By dc-biasing the common-drain HEMT near the gate-source pinch-off voltage, the second harmonic of the fundamental signal is generated due to HEMT nonlinearity. The phase difference between the S_2 and S_3 electrodes is 180° at the fundamental signal frequency, and 360° at the second harmonic frequency. By combining these signals in-phase at the S_2 and S_3 electrodes which are connected to each other, the fundamental output signals cancel out each other and the second harmonics arrive in-phase. At output port②, active impedance matching is achieved, due to the impedance-transition function of the common-drain HEMT; that is, from high to low. Since the common-drain HEMT is biased near the gate-source pinch-off voltage and driven by a large fundamental-frequency signal, active impedance matching is met by selecting the gate widths of gates G_2 and G_3, such that $g_2Z_0 = 1$ at the input fundamental frequency signal effective voltage, where g_2 is the conversion conductance [11] of the common-drain HEMT.

Measured magnitude and phase error versus input fundamental frequency characteristics of the line-unified common-gate HEMT and slotline series T-junction is shown in Fig. 5. The balanced performance of this part is mainly contributed to the fundamental-frequency signal suppression ratio (isolation) of the doubler. Magnitude error is the difference between the levels of each output port at the fundamental frequency. Phase error is the phase difference after subtracting 180°. As shown in the figure, the phase error is less than 12° in the frequency range from 2 GHz to 20 GHz, and the magnitude error is less than 2 dB above 7 GHz. These errors are small enough for a fundamental-frequency signal suppression ratio (isolation) of about 20 dB. [6]



(a)



(b)

Fig. 5. Measured magnitude and phase error versus input fundamental frequency characteristics of the line-unified common-gate HEMT and the slotline series T-junction. (a) Magnitude Error. (b) Phase Error.

III. Doubler Design

Assuming that the second harmonic is generated by the nonlinearity of the HEMT drain current (I_{ds}) versus gate-source voltage (V_{gs}), the conversion gain $G_C(2\omega)$ of the proposed doubler is given approximately by a quadratic function of the linear-state insertion gain $G_i(\omega)$ defined on one side of the balanced circuit, where ω is the input fundamental frequency. Therefore, the proposed doubler is designed by optimizing $G_i(\omega)$ characteristics through linear-state analysis. An analytic equivalent circuit diagram for the proposed balanced doubler is shown in Fig. 6.

Impedance $Z_L(\omega)$ mainly represents the inductances of L_1 and L_2. $V_{gd}(\omega)$, which represents the signal voltage between the gate and drain of the common-drain HEMT, is given by

$$V_{gd}(\omega) = Z(\omega)\, g_{m1} V_{\text{in}}(\omega) \tag{1}$$

with

$$Z(\omega) = \frac{Z_1(\omega) \cdot Z_2(\omega)}{Z_1(\omega) + 2Z_L(\omega) + 2Z_2(\omega)} \tag{2}$$

where g_{m1} is the transconductance of the common-gate HEMT, $V_{\text{in}}(\omega)$ is the fundamental frequency signal voltage at input port①, $Z_1(\omega)$ is the output impedance of the common-gate HEMT, and $Z_2(\omega)$ is the input impedance for each gate of the common-drain HEMT at the fundamental frequency. Since the common-gate HEMT is assumed to operate in a linear-state region, only $Z_2(\omega)$ is nonlinear in the right side of (2). When the equivalent circuit of the common-drain HEMT is represented in Fig.

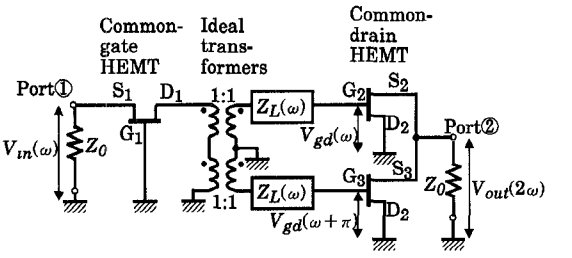


Fig. 6. Analytic equivalent circuit diagram of the proposed balanced frequency doubler.

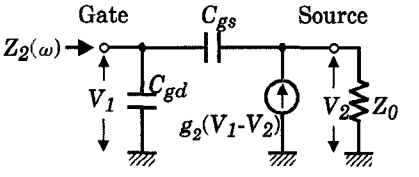


Fig. 7. Equivalent circuit of the common-drain HEMT terminated by Z_0.

7, $Z_2(\omega)$ is given by (3),

$$Z_2(\omega) = \frac{1 - g_2 Z_0 - j\omega C_{gs} Z_0}{j\omega C_{gd}(1 - g_2 Z_0) + j\omega C_{gs}(1 - j\omega C_{gd} Z_0)} \tag{3}$$

where C_{gs} and C_{gd} are gate-source and gate-drain capacitances, respectively. Applying the dc-bias condition $g_2 Z_0 = 1$, (3) becomes

$$Z_2(\omega) = \frac{-Z_0}{1 - j\omega C_{gd} Z_0} \tag{4}$$

Equations (1)–(4) show that the nonlinearity of $V_{gd}(\omega)$ depends on that of C_{gd}. The nonlinearity of C_{gd} is so small compared to that of I_{ds} versus V_{gs} characteristics [12] that the nonlinearity of I_{ds} versus V_{gs} characteristics is a dominant factor in the conversion gain of the doubler.

When HEMTs' dc I_{ds} versus V_{gs} characteristics for the saturation region given by (5) [12], the output magnitude voltage of the second harmonic signal, $V_{\text{out}}(2\omega)$, is given by (6),

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2\left(1 + \frac{V_{ds}}{R_{do} I_{dss}}\right) \quad \text{when } V_{gs} > V_p$$

$$I_{ds} = 0 \quad \text{when } V_{gs} \leqq V_p \tag{5}$$

where I_{dss} is the saturation current, V_p is the gate-source pinch-off voltage and R_{do} is the output conductance.

$$|V_{\text{out}}(2\omega)| = Z_0 \frac{I_{dss}}{2V_p^2}\left(1 + \frac{V_{ds}}{R_{do} I_{dss}}\right)|V_{gd}(\omega)|^2. \tag{6}$$

The details of the calculation of the $|V_{\text{out}}(2\omega)|$ are explicitly given in the Appendix. From (1) and (6), the conversion gain $G_C(2\omega)$ ($\equiv |V_{\text{out}}(2\omega)|^2/|V_{\text{in}}(\omega)|^2$) is given by

$$G_C(2\omega) = \left[Z_0 \frac{I_{dss}}{2V_p^2}\left(1 + \frac{V_{ds}}{R_{do} I_{dss}}\right) Z(\omega)^2 g_{m1}^2 |V_{\text{in}}(\omega)|\right]^2. \tag{7}$$

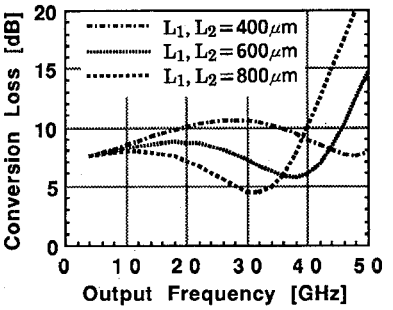


Fig. 8. Calculated conversion loss frequency responses versus length of the inductive lines L_1 and L_2.

On the other hand, when the common-drain HEMT is biased in the linear-state and the two source electrodes S_2, S_3 are disconnected each other, the linear-state insertion gain $G_i(\omega)$ from the S_1 to the S_2 or S_3 is approximately given by

$$G_i(\omega) \approx \left[\frac{g_{m2} Z_0}{1 + g_{m2} Z_0} Z(\omega) g_{m1} \right]^2 \tag{8}$$

where the g_{m2} is the transconductance of the common-drain HEMT biased in linear-state. From (7) and (8), the conversion gain $G_C(2\omega)$ is rewritten by

$$G_C(2\omega) \approx \left[Z_0 \frac{I_{dss}}{2V_p^2} \left(1 + \frac{V_{ds}}{R_{do} I_{dss}} \right) \cdot \left(\frac{1 + g_{m2} Z_0}{g_{m2} Z_0} \right)^2 |V_{\text{in}}(\omega)| \right]^2 G_i(\omega)^2. \tag{9}$$

All parameters on the right side of (9), except for $G_i(\omega)$, are constants for frequency ω. Therefore, the flat design of $G_i(\omega)$ provides wideband doubler operations. Fig. 8 shows calculated conversion loss frequency responses versus length of the inductive lines L_1 and L_2. By lengthening L_1 and L_2, the conversion loss is improved but the frequency bandwidth is reduced. 600 μm is chosen for the length of the inductive lines L_1, L_2.

IV. Experimental Results

A photograph and the measured performance of the MMIC balanced frequency doubler are shown in Figs. 9 and 10, respectively. The chip size is only 1.0 mm × 0.9 mm. This doubler has been fabricated using the n-AlGaAs/InGaAs HEMTs with a cutoff frequency of approximately 40 GHz. The gate length is 0.25 μm. The gate width of the common-gate HEMT and common-drain HEMT are 100 μm and two 50 μm wide gates, respectively.

The ultra-wideband characteristics of the doubler have been confirmed through on-wafer measurements up to an output frequency of 40 GHz, as shown in Fig. 10. Drain bias V_d(4 V) for the common-gate and common-drain HEMT is supplied through a dc pad. Source biases are supplied through a wideband bias T and on-wafer-measurement probes attached at input port ① and output port ②. The source bias of the common-gate HEMT is adjusted for a transconductance of approximately 20 mS, and the source bias of the common-drain HEMT is adjusted to near V_p for low conversion loss. The current drawn is typically 25 mA and the power consumption is 100 mW, when the input signal power is 6 dBm. The

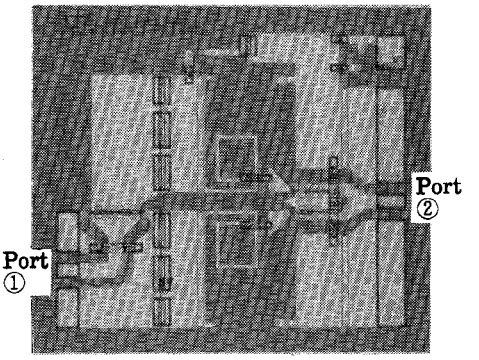
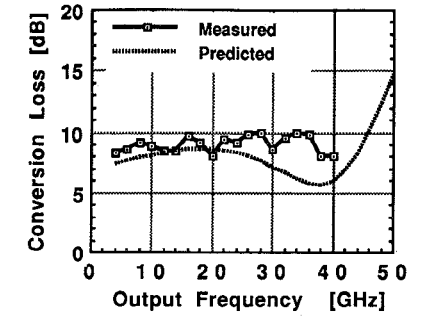


Fig. 9. Photograph of the fabricated MMIC balanced frequency doubler. The chip size is 1.0 mm × 0.9 mm.



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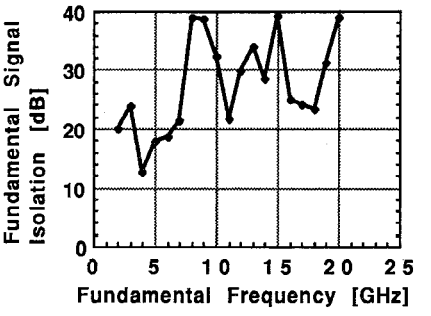

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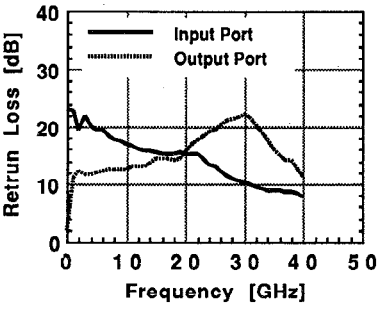

(c)

Fig. 10. Measured performance of the proposed MMIC balanced frequency doubler at an input power of 6 dBm. (a) Conversion loss frequency response. (b) Isolation frequency response. (c) Input and output return loss frequency response.

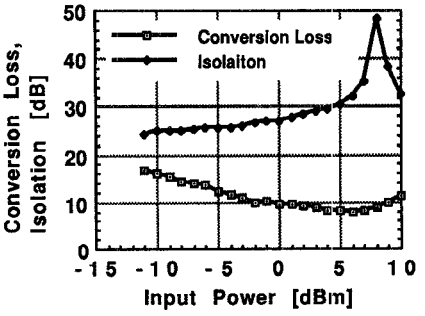

Fig. 11. Measured conversion loss and isolation performance as a function of input power at 10 GHz fundamental frequency.

measured performance is as follows: Conversion loss is 8–10 dB in the 4–40 GHz output frequency range; fundamental frequency signal isolation is better than 21 dB above an input fundamental frequency of 7 GHz; input return loss is better than 15 dB up to the input fundamental frequency of 20 GHz; output return loss is better than 12 dB in the 4–40 GHz output frequency range. The difference between measured and calculated conversion loss is mainly due to the neglect of the parastics caused by the MMIC pattern layouts. Below the input fundamental frequency of 5 GHz, the fundamental frequency signal isolation decreases due to the incomplete shift from the CPW mode to the slotline mode in the common-gate HEMT and the slotline series T-junction. The magnitude error of over 3 dB between 4 and 5 GHz in Fig. 4 causes an isolation of less than 20 dB When the area of the slotline and the slotline series T-junction is expanded, the isolation is improved.

The measured performance as a function of 10 GHz input power is shown in Fig. 11. Conversion loss decreases gradually as the input power increases and approaches the minimum value of 8 dB at an input power of 6 dBm. The fundamental frequency signal isolation increases gradually as the input power increases and exceeds 40 dB at an input power of 8 dBm.

V. Conclusion

A miniaturized, ultra-wideband MMIC balanced frequency doubler utilizing the line-unified HEMTs has been proposed and demonstrated through balanced phase- and magnitude error estimation and circuit parameter optimization using linear-state analysis. A conversion loss of 8–10 dB, an input return loss better than 15 dB and an output return loss better than 12 dB are obtained in the output frequency range from 4 to 40 GHz. The fundamental frequency signal isolation is better than 18 dB in the same output frequency range, except around 8 GHz. The proposed doubler promises to allow realization of miniaturized, wideband MMIC transmitters/receivers and multifunction MMICs.

Appendix

The output second harmonic signal voltage, $V_{out}(2\omega)$, formulated by (6), is derived from the dc drain current (5) and the analytic equivalent circuit diagram shown in Fig. 6. When attention is paid only to the fundamental signal voltage $V_{gd}(\omega)$ and the second harmonic signal voltage $V_{out}(2\omega)$ in (5), it is rewritten as

$$I_{ds} + i_{ds}(2\omega) = I_{dss}\left(1 - \frac{V_{gs} + V_{gd}(\omega) - V_{out}(2\omega)}{V_p}\right)^2 \cdot \left(1 + \frac{V_{ds} - V_{out}(2\omega)}{R_{do} I_{dss}}\right) \quad \text{(A1)}$$

for $V_{gs} + V_{gd}(\omega) - V_{out}(2\omega) > V_p$, which gives one cycle of the second harmonic. When rewriting $V_{gd}(\omega)$ and $V_{out}(2\omega)$ as follows:

$$V_{gd}(\omega) = |V_{gd}| \cos \omega t \quad \text{(A2)}$$

$$V_{out}(2\omega) = |V_{out}| \cos 2\omega t \quad \text{(A3)}$$

and applying the condition of bias $V_{gs} = V_p$ and $V_{out}(2\omega)/R_{do} I_{dss} \approx 0$, the second harmonic signal components of (A1) become

$$i_{ds}(2\omega) = \frac{I_{dss}}{2V_p^2}\left(1 + \frac{V_{ds}}{R_{do} I_{dss}}\right)|V_{gd}|^2 \cos 2\omega t. \quad \text{(A4)}$$

Therefore, $V_{out}(2\omega)$ is given by

$$V_{out}(2\omega) = Z_0 i_{ds}(2\omega) = Z_0 \frac{I_{dss}}{2V_p^2}\left(1 + \frac{V_{ds}}{R_{do} I_{dss}}\right)|V_{gd}|^2 \cos 2\omega t. \quad \text{(A5)}$$

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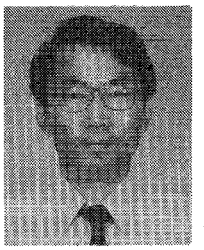

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